UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,029	09/24/2003	Mark Templeton	ARTCP047	7834

25920 7590 01/26/2005

MARTINE PENILLA & GENCARELLA, LLP
710 LAKEWAY DRIVE
SUITE 200
SUNNYVALE, CA 94085

EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,029	TEMPLETON ET AL.	
	Examiner	Art Unit	
	Sun J Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4-13* is/are allowed.

6)☒ Claim(s) *1,14,15,17 and 18* is/are rejected.

7)☒ Claim(s) *2,3,16 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/671,029 filed on 09/24/2003. Claims 1 – 19 remain pending in the application.

Specification Objections

2 The specification is objected to because of following informalities:

Page 3, Paragraph 0006, line 3, change "specification" to **—specification.—**.

Appropriate correction is required.

Drawing Objections

3. Drawing listed below is objected to because of following informalities:

Fig. 1 should be labeled as a —(PRIOR ART)—.

Appropriate correction is required.

Claim Objections

4. Claims listed below are objected to because of the following informalities:

Claim 1, line 3, after "improving" delete **—the—**.
Claim 1, line 4, change "process" to **—environment—**.
Claim 1, line 6, change "the library" to **—a library—**.
Claim 1, line 8, after "selecting" insert **—standard cells in—**.
Claim 1, line 9, before "yield" delete **—resulting—**.
Claim 3, line 1, change "the variants ... manufacturability" to **—each of the variants is assigned a manufacturability rating—**.
Claim 4, line 2 (2 places), change "the integrated" to **—an integrated—**.
Claim 4, line 6, before "designer's" delete **—the—**.
Claim 5, line 1, before "standard" delete **—cells of—**.
Claim 6, line 1, before "standard" delete **—cells of—**.
Claim 7, line 1, before "standard" delete **—cells of—**.
Claim 7, line 2, before "core" delete **—the—**.
Claim 8, line 1, before "standard" delete **—cells of—**.
Claim 8, line 1, change "least a" to **—least an—**.

Claim 8, line 2, before "analog" delete —**first**—.

Claim 9, line 2, before "components" insert —**standard**—.

Claim 12, line 2, before "manufacturing" delete —**first**—.

Claim 14, line 1, before "manufacturability" delete —**the**—.

Claim 14, line 1, change "integrated circuits" to —**an integrated circuit**—.

Claim 14, line 5, after "problem:" insert —**and**—.

Claim 14, line 6, change "a design synthesis tool" to —**a synthesis tool**—.

Claim 14, line 7, change "a proposed IC designs" to —**a proposed IC design**—.

Claim 14, line 8, change "the particular" to —**a particular**—.

Claim 16, line 3, change "may be" to —**is**—.

Claim 19, line 2, change "yield limiters" to —**IC yield limiter**—.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1, 14, 15, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Applicants' Admitted Prior Art* (Fig. 1; Fig. 2; Paragraph 0002 – 0008] in view of U.S. Patent Application Publication No. 2004/0143797 A1 to *Nguyen et al.* over U.S. Patent No. 6,418,353 B1 to *Rostoker et al.*

7. As to Claim 1, *Applicants' Admitted Prior Art* (called *AAPA* hereinafter) shows and teaches the following subject matter:

- Design flow for logic functions within in IC – [Fig. 2];
- A *library of standard cells* 55 (i.e., *standard cell library*) consists a plurality of *different cell types* (e.g., AND, NOR, flip-flop and INV *standard logic cells*); each cell will be available in several *different sizes* – [Fig. 2; Paragraph 0005];
- IC designer is typically provide with *multiple variants* of each hard macro, the *variants* showing different *trade off* among the variables of area, speed and power – [Paragraph 0008]; Notice that (1) a *hard macro* is a *standard cell performing a specific function* (2) multiple variants of standard cells are stored in a library (e.g., standard cell library).

AAPA teaches designing and providing a plurality of different variants for standard cells in a library, but *AAPA* doest not teach a method of addressing *manufacturing problem* for each of *standard cell variant*. But *Nguyen et al.* teach providing a *standard cell library* having *layout architecture* that is designed for *fabrication technologies* (i.e., *manufacturing technologies*) having *design rules* of *0.12 microns or smaller* – [abstract]. Notice that (1) IC's which are 0.12 microns and larger have different *layout architectures*, they are built using *different standard cell variants* due to *different fabrication technologies* (2) *different fabrication technologies* have *different manufacturing environments* (3) *different standard cell variants* are utilized to meet *different design rules* associated with *different fabrication technologies* (4) the *design rule* addresses *requirements* associated with *manufacturing problem* needed to be considered in manufacturing a desired design using a specific *fabrication technologies*.

It is also noticed that a *standard cell variant* addressing *design rule* regarding requirements associated with *manufacturing problem* provides designer useful information in selecting standard cells contained in an appropriate *standard cell variant* for use in fabrication of integrated circuits to implement desired logic functions in a specific manufacturing environment.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Nguyen et al.* in

addressing *design rule* regarding *requirements* associated with *manufacturing problem* for each *standard cell variant* in order to provide designer useful information in selecting standard cells contained in an appropriate *standard cell variant* for use in fabrication of integrated circuits to implement desired logic functions in a specific manufacturing environment.

AAPA and *Nguyen et al.* teach all subject matter given above, they do not teach a method of selecting standard cells in one standard cell variant in order to optimize yield of integrated circuits in a particular manufacturing environment. But *Rostoker et al.* teach a method of performing trade-off analysis in order to utilizing *larger minimum device size* in order to achieve a *higher yield* in a particular *manufacture process* (i.e., *manufacturing environment*) – [col. 4, line 50 – col. 5, line 31]. *Rostoker et al.* also teach (1) determining minimum feature size, based on manufacturing information resulting in yield data in wafer (fabrication process), in manufacturing an integrated circuit – [abstract] (2) *numerical aperture library* (e.g., *standard cell library*) for use in design of mask – [col. 5, line 40 – 50].

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Rostoker et al.* in performing trade-off analysis in order to utilizing *larger minimum device size* of standard cells in a standard cell variant in order to achieve a *higher yield* in a particular *manufacturing environment*.

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

8. As to Claim 14, in addition to reasons include in **[Response A]** given above, *AAPA*, *Nguyen et al.* and *Rostoker et al.* in show and teach the following subject matter:

- a *library* comprised a plurality of *variant designs* for *standard components* – [*Nguyen et al.*: abstract; Fig. 6; **Response A**]
- a *synthesis tool 53* coupled to a *standard cell library 55* formulating and presenting to a user a *netlist 57* of a proposed IC design – [*AAPA*: Fig. 2];
- A design incorporating a *variant design* (i.e., larger minimum device sizes) that corrects a *known manufacturing problem* due to constraints of lithography

module in a particular *manufacturing environment* (i.e., *wafer process*) in order to achieve higher yield – [*Rostoker et al.*: **Response A**].

9. As to Claim 15, reasons are included in **[Response A]** given above.

10. As to Claim 17, *Nguyen et al.* show the subject matter in Fig. 6.

11. As to Claim and 18, in addition to reasons included in **[Response A]**, AAPA shows in Fig. 1 that *I/O cells 18* (i.e., *input/output cells*) are *standard components* of a logic integrated circuit. Notice that a buffer cell, which is made of inverter(s), can be served as a input/output cell.

Allowable Subject Matter

12. Claims 4 – 13 are allowed. Claims 2, 3, 16 and 19 are objected to as being dependent upon a rejected base claim, but they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Those claims are allowed is because that the prior art does not teach or fairly suggest the following subject matter:

- A method for allowing an integrated circuit designer to optimize an integrated circuit design, the method comprising the steps of *designing a plurality of variants of standard components*, *rating each design variant on at least one variable* and *selecting the design variant whose rating most closely matches designer's criteria for use in the integrated circuit design* as recited in independent **Claim 4**;
- Variants are designed to at least address the manufacturing problems of *poor contact formation*, *contact alignment*, *metal line spacing* and *metal line direction changes* as recited in **Claim 2**;
- Each of variants is assigned a manufacturability rating and selecting a standard cell variant is influenced by the assigned manufacturability rating as recited in **Claim 3**;

- Variant designs of standard logic cells are rated on a *manufacturability index*, a different rating being assigned to each variant for each manufacturing environment in which it is used as recited in **Claim 16**;
- Variant designs include compensation for a design related *IC yield limiters*, the *IC yield limiter including at least leakage current through transistors* as recited in **Claim 19**.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272 - 1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin
Patent Examiner
Art Unit 2825
January 24, 2005